Abstract

Ultra-low power basic blocks and their uses

The present invention relates to ultra-low power (ULP) electronic circuits which do not dissipate more than 10 µW, preferably not more than 1 µW. An ultra-low power device comprising a series connection of an n-MOS transistor and a p-MOS transistor each having a source and a drain, whereby the source of the n-MOS transistor is coupled with the source of the p-MOS transistor is provided. Both transistors are such that the absolute values of their threshold voltages are different, and that the absolute value of the relative difference of both threshold voltages is between 0.9 and 1.3 Volts. Each of the transistors in the ultra-low power device having at least one gate, these gates may be coupled together to form a common gate. Different applications of these basic blocks are given, such as ULP reference voltage, a ULP level shifter, a ULP voltage multiplier, a ULP OTA. Also a new diode is described.

+ Fig. 7